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EXAMINER	
GANDHI, DIPAKKUMAR B	
ART UNIT	PAPER NUMBER
2117	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/712,660	WEINRAUB, CHANANIEL	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because in figure 4, item number "71" should be "update register inside the control BSR" as per page 7, line 12 of the specification. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: In line 3, page 1 of the specification, "Attorney Docket no. TI-35491PS" should be removed.

Appropriate correction is required.

3. The disclosure is objected to because of the following informalities: In lines 23-24 of page 7 of the specification, "period" is missing at the end of the sentence.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 12 is rejected under 35 U.S.C. 102(b) as being anticipated by Whetsel (US 5,701,307).

Whetsel anticipates claim 12.

Whetsel teaches a protection circuit operational to prevent damage to a good device during JTAG final testing of a circuit board that employs the good device ("The IEEE 1149.1 standard defines three types of test operations for boundary scan cells, a sample test operation (Sample), an external test (Extest) and internal test (Intest)", col. 1, lines 62-64, Whetsel. "Extest is another required test mode for 1149.1. During Extest, output boundary scan cells are used to drive test data from IC outputs onto wiring interconnects, and input boundary scan cells are used to capture the driven test data at IC inputs. In this way, Extest can be used to test wiring interconnects between IC inputs and outputs on a board. Intest is an optional test mode for 1149.1. During Intest, input boundary scan cells are used to drive test data to the IC's core logic, and output boundary scan cells are used to capture the response from the core logic. In this way, Intest can be used to test IC core logic", col. 2, lines 2-12, Whetsel. "Using the boundary scan cells of the present invention in FIGS. 4 and 6, the latchable output buffer 40, when used in combination with the momentary control method of Control 2 (FIG. 4) or Control 2 and Transfer (FIG. 6), significantly reduces the time an output buffer can be forced into a short circuit condition. For example, the Control 2 or Control 2 and Transfer signals can be made to momentarily enable TG2 or TG2 and TG3 for only one half TCK period during update. After the momentary update enable goes away, the latch buffer provides feedback to correct for any output short condition immediately. In comparing short circuit correction times between the boundary scan cell of FIG. 3 (4 TCK periods) and those of FIGS. 4 and 6 (1/2 TCK period), the cells of the present invention correct shorts in 12.5% of the time it takes the prior art cell to correct shorts. Therefore the invention reduces the potential for output buffers to be degraded or destroyed during Extest or Intest operation", col. 10, lines 7-23, Whetsel. "A short circuit test procedure and protection method for newly assembled boards or multi-chip modules; a Disable feature to allow IC output pins to go to non-conflicting states on power up; testing for shorts prior to enabling the IC to enter normal operation; a sequence of steps at power up to insure that no shorts exist on IC output pins; and feedback

designed into the IC output buffer; and the ability to disable the core logic output to enable safe IC power up even with outputs shorted", col. 13, line 67 to col. 14, line 8, Whetsel). IEEE Std. 1149.1 is IEEE Standard Test Access Port and Boundary-Scan Architecture. The examiner would like to point out that by correcting shorts in a very short time it prevents damage to a good device during testing.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

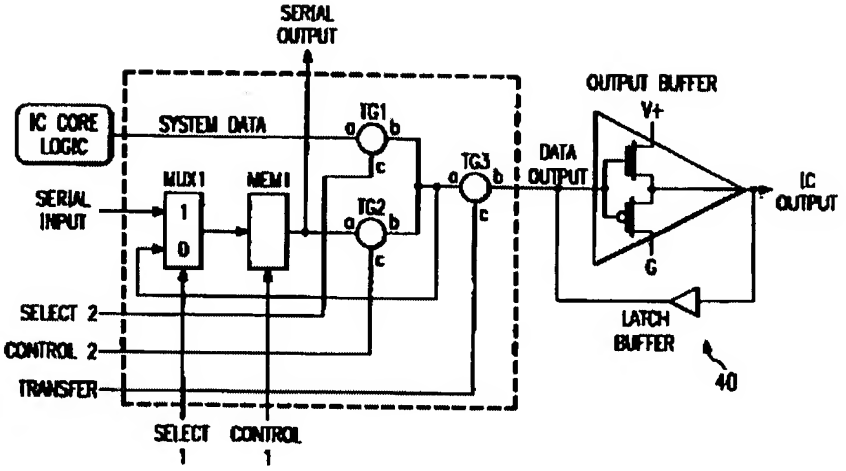
1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 1-11, 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Whetsel (US 5,701,307) in view of Tsai et al. (US 5,570,375) and Boomer (US 5,256,914).

As per claim 1, Whetsel teaches an integrated circuit (IC) device outputs test protection circuit comprising: a test protection circuit register responsive to the first logic signal, a test clock and a TAP controller instruction to generate a second logic signal; and logic circuitry responsive to at least one BSR signal and the second logic signal to generate a protection circuit output control signal, wherein the protection circuit output control signal operates within one test clock cycle to disable circuit output associated with a short circuit corresponding to the IC device ("The invention relates to integrated circuits (ICs) and, more particularly, to boundary scan cells implemented at input and output pins of ICs to simplify testing of the ICs and their wiring interconnections", col. 1, lines 22-25, Whetsel. "Using the boundary scan cells of the

present invention in FIGS. 4 and 6, the latchable output buffer 40, when used in combination with the momentary control method of Control 2 (FIG. 4) or Control 2 and Transfer (FIG. 6), significantly reduces the time an output buffer can be forced into a short circuit condition. For example, the Control 2 or Control 2 and Transfer signals can be made to momentarily enable TG2 or TG2 and TG3 for only one half TCK period during update. After the momentary update enable goes away, the latch buffer provides feedback to correct for any output short condition immediately. In comparing short circuit correction times between the boundary scan cell of FIG. 3 (4 TCK periods) and those of FIGS. 4 and 6 (1/2 TCK period), the cells of the present invention correct shorts in 12.5% of the time it takes the prior art cell to correct shorts. Therefore the invention reduces the potential for output buffers to be degraded or destroyed during Extest or Intest operation. The reason for this improved short circuit protection provided by the invention is that the latchable output buffer 40 immediately and asynchronously corrects for logic differences between the input and the output of the output buffer using the latch buffer as a feedback mechanism", fig. 4, 6, col. 10, lines 7-28, Whetsel. "A short circuit test procedure and protection method for newly assembled boards or multi-chip modules; a Disable feature to allow IC output pins to go to non-conflicting states on power up; testing for shorts prior to enabling the IC to enter normal operation; a sequence of steps at power up to insure that no shorts exist on IC output pins; and feedback designed into the IC output buffer; and the ability to disable the core logic output to enable safe IC power up even with outputs shorted", col. 13, line 67 to col. 14, line 8, Whetsel).

FIG. 6



However Whetsel does not explicitly teach the specific use of decision circuitry responsive to predetermined boundary scan register (BSR) signals and a test access port (TAP) controller mode signal to generate a first logic signal.

Tsai et al. in an analogous art teach the boundary scan registers and the TAP controller (col. 3, lines 21-22, Tsai et al.). Tsai et al. also teach that the XOR gate 44 has a first input, which serves as a feedback input fb, a second input, which serves as a scan input, and an output (fig. 8, col. 6, lines 47-49, Tsai et al.).

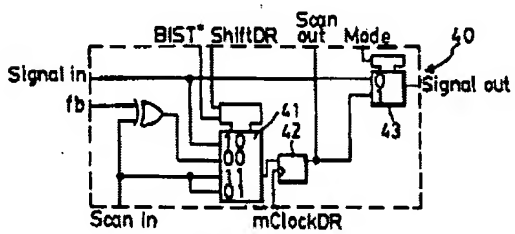


FIG.8

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Whetsel's patent with the teachings of Tsai et al. by including an additional step of using decision circuitry responsive to predetermined boundary scan register (BSR) signals and a test access port (TAP) controller mode signal to generate a first logic signal.

This modification would have been obvious to one of ordinary skill the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to detect a short circuit or overload at the output buffer.

Whetsel also does not explicitly teach the specific use of disabling an output buffer associated with a short circuit corresponding to the IC device.

However Boomer in an analogous art teaches that the step of tristating the output buffer circuit is accomplished by logically processing the short circuit sensing signal, generating a short circuit tristate enable signal SOEB, and coupling the short circuit tristate enable signal to the tristate enable input of the existing tristate enable circuit for tristating (i.e. disabling) the output buffer circuit (col. 2, lines 51-57, Boomer).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Whetsel's patent with the teachings of Boomer by including an additional step of disabling an output buffer associated with a short circuit corresponding to the IC device.

This modification would have been obvious to one of ordinary skill the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that disabling an output buffer associated with a short circuit corresponding to the IC device would provide the opportunity to protect a good device connected to the IC device when short circuit occurs.

- As per claim 2, Whetsel, Tsai et al. and Boomer teach the additional limitations.

Whetsel teaches that the predetermined BSR signals comprise a primary input buffer signal, an output BSR signal and a control BSR update register control signal ("FIGS. 4 and 6 illustrate exemplary output boundary scan cells according to the invention", col. 5, lines 24-25, Whetsel. "During Extest operation, the boundary scan cell receives Select 1 and Control 1 input to capture the IC output pin data into Mem1 and then shift it out for inspection via the serial output", col. 6, lines 52-55, Whetsel. "During Intest operation,

Mux1 is controlled to input system data from the output of the latchable input buffer 103 to Mem1 for capturing and shifting out", fig. 15, col. 14, line 67 to col. 15, line 3, Whetsel).

- As per claim 3, Whetsel, Tsai et al. and Boomer teach the additional limitations.

Tsai et al. teach that the decision circuitry comprises exclusive OR circuitry operational to receive the primary input buffer signal and the output BSR signal ("The XOR gate 44 has a first input, which serves as a feedback input fb, a second input, which serves as a scan input, and an output", fig. 8, col. 6, lines 47-49, Tsai et al.).

- As per claim 4, Whetsel, Tsai et al. and Boomer teach the additional limitations.

Tsai et al. teach that the test protection circuit register is further responsive to a previous protection data register (DR) associated with a corresponding protection DR chain to generate the second logic signal ("Test Data In (TDI) which provides serial inputs for test instructions shifted into the instruction register and for data shifted through the boundary-scan register or other test data registers", fig. 5, col. 2, lines 29-32, Tsai et al.).

- As per claim 5, Whetsel, Tsai et al. and Boomer teach the additional limitations.

Whetsel teaches an integrated circuit (IC) device outputs test protection circuit comprising: means responsive to the first logic signal, a test clock and a TAP controller instruction for generating a second logic signal; and means responsive to at least one BSR signal and the second logic signal for generating a protection circuit output control signal, wherein the protection circuit output control signal operates within one test clock cycle to disable circuit output associated with a short circuit corresponding to the IC device ("The invention relates to integrated circuits (ICs) and, more particularly, to boundary scan cells implemented at input and output pins of ICs to simplify testing of the ICs and their wiring interconnections", col. 1, lines 22-25, Whetsel. "Using the boundary scan cells of the present invention in FIGS. 4 and 6, the latchable output buffer 40, when used in combination with the momentary control method of Control 2 (FIG. 4) or Control 2 and Transfer (FIG. 6), significantly reduces the time an output buffer can be forced into a short circuit condition. For example, the Control 2 or Control 2 and Transfer signals can be made to momentarily enable TG2 or TG2 and TG3 for only one half TCK period during update. After the momentary update enable goes away, the latch buffer provides feedback to correct for

any output short condition immediately. In comparing short circuit correction times between the boundary scan cell of FIG. 3 (4 TCK periods) and those of FIGS. 4 and 6 (1/2 TCK period), the cells of the present invention correct shorts in 12.5% of the time it takes the prior art cell to correct shorts. Therefore the invention reduces the potential for output buffers to be degraded or destroyed during Extest or Intest operation. The reason for this improved short circuit protection provided by the invention is that the latchable output buffer 40 immediately and asynchronously corrects for logic differences between the input and the output of the output buffer using the latch buffer as a feedback mechanism", fig. 4, 6, col. 10, lines 7-28, Whetsel).

Tsai et al. teach means responsive to predetermined boundary scan register (BSR) signals and a test access port (TAP) controller mode signal for generating a first logic signal ("The boundary scan registers and the TAP controller", col. 3, lines 21-22, Tsai et al. "The XOR gate 44 has a first input, which serves as a feedback input fb, a second input, which serves as a scan input, and an output", fig. 8, col. 6, lines 47-49, Tsai et al.).

Boomer teaches disabling an output buffer associated with a short circuit corresponding to the IC device ("The step of tristating the output buffer circuit is accomplished by logically processing the short circuit sensing signal, generating a short circuit tristate enable signal SOEB, and coupling the short circuit tristate enable signal to the tristate enable input of the existing tristate enable circuit for tristating (i.e. disabling) the output buffer circuit", col. 2, lines 51-57, Boomer).

- As per claim 6, Whetsel, Tsai et al. and Boomer teach the additional limitations.

Tsai et al. teach that the means for generating a first logic signal comprises decision circuitry ("The XOR gate 44 has a first input, which serves as a feedback input fb, a second input, which serves as a scan input, and an output", fig. 8, col. 6, lines 47-49, Tsai et al.).

- As per claim 7, Whetsel, Tsai et al. and Boomer teach the additional limitations.

Whetsel teaches that the means for generating a second logic signal comprises a test protection circuit register ("If a short to ground existed on the IC output pin and the momentary control method were used to transfer a logic one from Mem1 to the latchable output buffer 40, the latchable output buffer would temporarily force (during the Control 2 or Control 2 and Transfer time) the output to a logic one.

However, after the momentary control goes away, the latchable output buffer 40 would, due to the output feedback from the latch buffer, immediately switch from outputting a logic one to outputting a logic zero, thus removing the voltage contention at the IC output pin", col. 9, lines 30-39, Whetsel). The examiner would like to point out that Mem1 is a capture/shift memory such as a flip-flop, col. 1, line 35, Whetsel.

- As per claim 8, Whetsel, Tsai et al. and Boomer teach the additional limitations.

Tsai et al. teach that the test protection circuit register is further responsive to a previous protection data register (DR) associated with a corresponding protection DR chain to generate the second logic signal ("Test Data In (TDI) which provides serial inputs for test instructions shifted into the instruction register and for data shifted through the boundary-scan register or other test data registers", fig. 5, col. 2, lines 29-32, Tsai et al.).

- As per claim 9, Whetsel, Tsai et al. and Boomer teach the additional limitations.

Whetsel teaches that the means for generating a protection circuit output control signal comprises logic circuitry ("Using the boundary scan cells of the present invention in FIGS. 4 and 6, the latchable output buffer 40, when used in combination with the momentary control method of Control 2 (FIG. 4) or Control 2 and Transfer (FIG. 6), significantly reduces the time an output buffer can be forced into a short circuit condition. For example, the Control 2 or Control 2 and Transfer signals can be made to momentarily enable TG2 or TG2 and TG3 for only one half TCK period during update. After the momentary update enable goes away, the latch buffer provides feedback to correct for any output short condition immediately. In comparing short circuit correction times between the boundary scan cell of FIG. 3 (4 TCK periods) and those of FIGS. 4 and 6 (1/2 TCK period), the cells of the present invention correct shorts in 12.5% of the time it takes the prior art cell to correct shorts. Therefore the invention reduces the potential for output buffers to be degraded or destroyed during Extest or Intest operation. The reason for this improved short circuit protection provided by the invention is that the latchable output buffer 40 immediately and asynchronously corrects for logic differences between the input and the output of the output buffer using the latch buffer as a feedback mechanism", fig. 4, 6, col. 10, lines 7-28, Whetsel).

- As per claim 10, Whetsel, Tsai et al. and Boomer teach the additional limitations.

Whetsel teaches that the predetermined BSR signals comprise a primary input buffer signal, an output BSR signal and a control BSR update register control signal ("FIGS. 4 and 6 illustrate exemplary output boundary scan cells according to the invention", col. 5, lines 24-25, Whetsel. "During Extest operation, the boundary scan cell receives Select 1 and Control 1 input to capture the IC output pin data into Mem1 and then shift it out for inspection via the serial output", col. 6, lines 52-55, Whetsel. "During Intest operation, Mux1 is controlled to input system data from the output of the latchable input buffer 103 to Mem1 for capturing and shifting out", fig. 15, col. 14, line 67 to col. 15, line 3, Whetsel).

- As per claim 11, Whetsel, Tsai et al. and Boomer teach the additional limitations.

Tsai et al. teach that the means for generating a first logic signal comprises exclusive OR circuitry operational to receive the primary input buffer signal and the output BSR signal ("The XOR gate 44 has a first input, which serves as a feedback input fb, a second input, which serves as a scan input, and an output", fig. 8, col. 6, lines 47-49, Tsai et al.).

- As per claim 26, Whetsel, Tsai et al. and Boomer teach the additional limitations.

Whetsel teaches that a method of providing integrated circuit (IC) device outputs protection during JTAG board tests, the method comprising the steps of: providing an IC device outputs test protection circuit; a test protection circuit register responsive to the first logic signal, a test clock and a TAP controller instruction to generate a second logic signal; and logic circuitry responsive to at least one BSR signal and the second logic signal to generate a protection circuit output control signal; and generating the protection circuit output control signal within one test clock cycle to disable circuit output associated with a short circuit condition or overload condition corresponding to an IC device ("The invention relates to integrated circuits (ICs) and, more particularly, to boundary scan cells implemented at input and output pins of ICs to simplify testing of the ICs and their wiring interconnections", col. 1, lines 22-25, Whetsel. "The IEEE 1149.1 standard defines three types of test operations for boundary scan cells, a sample test operation (Sample), an external test (Extest) and internal test (Intest)", col. 1, lines 62-64, Whetsel. "Extest is another required test mode for 1149.1. During Extest, output boundary scan cells are used to drive test data from IC outputs onto wiring interconnects, and input boundary scan cells are used to capture the driven test data at IC inputs. In this way, Extest can be used to test wiring interconnects between IC

inputs and outputs on a board. Intest is an optional test mode for 1149.1. During Intest, input boundary scan cells are used to drive test data to the IC's core logic, and output boundary scan cells are used to capture the response from the core logic. In this way, Intest can be used to test IC core logic", col. 2, lines 2-12, Whetsel. "Using the boundary scan cells of the present invention in FIGS. 4 and 6, the latchable output buffer 40, when used in combination with the momentary control method of Control 2 (FIG. 4) or Control 2 and Transfer (FIG. 6), significantly reduces the time an output buffer can be forced into a short circuit condition. For example, the Control 2 or Control 2 and Transfer signals can be made to momentarily enable TG2 or TG2 and TG3 for only one half TCK period during update. After the momentary update enable goes away, the latch buffer provides feedback to correct for any output short condition immediately. In comparing short circuit correction times between the boundary scan cell of FIG. 3 (4 TCK periods) and those of FIGS. 4 and 6 (1/2 TCK period), the cells of the present invention correct shorts in 12.5% of the time it takes the prior art cell to correct shorts. Therefore the invention reduces the potential for output buffers to be degraded or destroyed during Extest or Intest operation. The reason for this improved short circuit protection provided by the invention is that the latchable output buffer 40 immediately and asynchronously corrects for logic differences between the input and the output of the output buffer using the latch buffer as a feedback mechanism", fig. 4, 6, col. 10, lines 7-28, Whetsel. "A short circuit test procedure and protection method for newly assembled boards or multi-chip modules; a Disable feature to allow IC output pins to go to non-conflicting states on power up; testing for shorts prior to enabling the IC to enter normal operation; a sequence of steps at power up to insure that no shorts exist on IC output pins; and feedback designed into the IC output buffer; and the ability to disable the core logic output to enable safe IC power up even with outputs shorted", col. 13, line 67 to col. 14, line 8, Whetsel).

Tsai et al. teach decision circuitry responsive to predetermined boundary scan register (BSR) signals and a test access port (TAP) controller mode signal to generate a first logic signal ("The boundary scan registers and the TAP controller", col. 3, lines 21-22, Tsai et al. "The XOR gate 44 has a first input, which serves as a feedback input fb, a second input, which serves as a scan input, and an output", fig. 8, col. 6, lines 47-49, Tsai et al.).

Boomer teaches disabling an output buffer associated with a short circuit condition or overload condition corresponding to an IC device ("The step of tristating the output buffer circuit is accomplished by logically processing the short circuit sensing signal, generating a short circuit tristate enable signal SOEB, and coupling the short circuit tristate enable signal to the tristate enable input of the existing tristate enable circuit for tristating (i.e. disabling) the output buffer circuit", col. 2, lines 51-57, Boomer).

9. Claims 13, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Whetsel (US 5,701,307) as applied to claim 12 above, and further in view of Boomer (US 5,256,914).

As per claim 13, Whetsel substantially teach the claimed invention described in claim 12 (as rejected above). Whetsel teaches logic circuitry responsive to predetermined BSR signals to generate a protection circuit output control signal that operates within one test clock cycle to disable output circuit associated with a short circuit or overload condition corresponding to the good device ("Using the boundary scan cells of the present invention in FIGS. 4 and 6, the latchable output buffer 40, when used in combination with the momentary control method of Control 2 (FIG. 4) or Control 2 and Transfer (FIG. 6), significantly reduces the time an output buffer can be forced into a short circuit condition. For example, the Control 2 or Control 2 and Transfer signals can be made to momentarily enable TG2 or TG2 and TG3 for only one half TCK period during update. After the momentary update enable goes away, the latch buffer provides feedback to correct for any output short condition immediately. In comparing short circuit correction times between the boundary scan cell of FIG. 3 (4 TCK periods) and those of FIGS. 4 and 6 (1/2 TCK period), the cells of the present invention correct shorts in 12.5% of the time it takes the prior art cell to correct shorts. Therefore the invention reduces the potential for output buffers to be degraded or destroyed during Extest or Intest operation. The reason for this improved short circuit protection provided by the invention is that the latchable output buffer 40 immediately and asynchronously corrects for logic differences between the input and the output of the output buffer using the latch buffer as a feedback mechanism", fig. 4, 6, col. 10, lines 7-28, Whetsel. "A short circuit test procedure and protection method for newly assembled boards or multi-chip modules; a Disable feature to allow IC output pins to go to non-conflicting states on power up; testing for shorts prior to enabling the IC to enter normal operation; a sequence of steps at power up to insure that no shorts exist on IC output pins; and feedback designed

into the IC output buffer; and the ability to disable the core logic output to enable safe IC power up even with outputs shorted", col. 13, line 67 to col. 14, line 8, Whetsel).

However Whetsel does not explicitly teach the specific use of disabling an output buffer associated with a short circuit or overload condition corresponding to the good device.

Boomer in an analogous art teaches that the step of tristating the output buffer circuit is accomplished by logically processing the short circuit sensing signal, generating a short circuit tristate enable signal SOEB, and coupling the short circuit tristate enable signal to the tristate enable input of the existing tristate enable circuit for tristating (i.e. disabling) the output buffer circuit (col. 2, lines 51-57, Boomer).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Whetsel's patent with the teachings of Boomer by including an additional step of disabling an output buffer associated with a short circuit or overload condition corresponding to the good device. This modification would have been obvious to one of ordinary skill the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that disabling an output buffer associated with a short circuit or overload condition corresponding to the good device would provide the opportunity to protect a good device connected to the IC device when short circuit occurs.

- As per claim 14, Whetsel and Boomer teach the additional limitations.

Whetsel teaches that the predetermined BSR signals comprise a primary input buffer signal, an output BSR signal and a control BSR update register control signal ("FIGS. 4 and 6 illustrate exemplary output boundary scan cells according to the invention", col. 5, lines 24-25, Whetsel. "During Extest operation, the boundary scan cell receives Select 1 and Control 1 input to capture the IC output pin data into Mem1 and then shift it out for inspection via the serial output", col. 6, lines 52-55, Whetsel. "During Intest operation, Mux1 is controlled to input system data from the output of the latchable input buffer 103 to Mem1 for capturing and shifting out", fig. 15, col. 14, line 67 to col. 15, line 3, Whetsel).

10. Claims 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Whetsel (US 5,701,307) as applied to claim 12 above, and further in view of Tsai et al. (US 5,570,375) and Boomer (US 5,256,914).

As per claim 15, Whetsel substantially teach the claimed invention described in claim 12 (as rejected above). Whetsel further teaches a test protection circuit register responsive to the first logic signal, a test clock and a TAP controller instruction to generate a second logic signal; and logic circuitry responsive to at least one BSR signal and the second logic signal to generate a protection circuit output control signal, wherein the protection circuit output control signal operates within one test clock cycle to disable circuit output associated with a short circuit corresponding to the IC device ("The invention relates to integrated circuits (ICs) and, more particularly, to boundary scan cells implemented at input and output pins of ICs to simplify testing of the ICs and their wiring interconnections", col. 1, lines 22-25, Whetsel. "Using the boundary scan cells of the present invention in FIGS. 4 and 6, the latchable output buffer 40, when used in combination with the momentary control method of Control 2 (FIG. 4) or Control 2 and Transfer (FIG. 6), significantly reduces the time an output buffer can be forced into a short circuit condition. For example, the Control 2 or Control 2 and Transfer signals can be made to momentarily enable TG2 or TG2 and TG3 for only one half TCK period during update. After the momentary update enable goes away, the latch buffer provides feedback to correct for any output short condition immediately. In comparing short circuit correction times between the boundary scan cell of FIG. 3 (4 TCK periods) and those of FIGS. 4 and 6 (1/2 TCK period), the cells of the present invention correct shorts in 12.5% of the time it takes the prior art cell to correct shorts. Therefore the invention reduces the potential for output buffers to be degraded or destroyed during Extest or Intest operation. The reason for this improved short circuit protection provided by the invention is that the latchable output buffer 40 immediately and asynchronously corrects for logic differences between the input and the output of the output buffer using the latch buffer as a feedback mechanism", fig. 4, 6, col. 10, lines 7-28, Whetsel. "A short circuit test procedure and protection method for newly assembled boards or multi-chip modules; a Disable feature to allow IC output pins to go to non-conflicting states on power up; testing for shorts prior to enabling the IC to enter normal operation; a sequence of steps at power up to insure that no shorts exist on IC output pins; and feedback designed into the IC output buffer; and the ability to disable the core logic output to enable safe IC power up even with outputs shorted", col. 13, line 67 to col. 14, line 8, Whetsel).

However Whetsel does not explicitly teach the specific use of decision circuitry responsive to predetermined boundary scan register (BSR) signals and a test access port (TAP) controller mode signal to generate a first logic signal.

Tsai et al. in an analogous art teach the boundary scan registers and the TAP controller (col. 3, lines 21-22, Tsai et al.). Tsai et al. also teach that the XOR gate 44 has a first input, which serves as a feedback input fb, a second input, which serves as a scan input, and an output (fig. 8, col. 6, lines 47-49, Tsai et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Whetsel's patent with the teachings of Tsai et al. by including an additional step of using decision circuitry responsive to predetermined boundary scan register (BSR) signals and a test access port (TAP) controller mode signal to generate a first logic signal.

This modification would have been obvious to one of ordinary skill the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to detect a short circuit or overload at the output buffer.

Whetsel also does not explicitly teach the specific use of disabling an output buffer associated with a short circuit corresponding to the IC device.

However Boomer in an analogous art teaches that the step of tristating the output buffer circuit is accomplished by logically processing the short circuit sensing signal, generating a short circuit tristate enable signal SOEB, and coupling the short circuit tristate enable signal to the tristate enable input of the existing tristate enable circuit for tristating (i.e. disabling) the output buffer circuit (col. 2, lines 51-57, Boomer).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Whetsel's patent with the teachings of Boomer by including an additional step of disabling an output buffer associated with a short circuit corresponding to the IC device.

This modification would have been obvious to one of ordinary skill the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that disabling an output buffer

associated with a short circuit corresponding to the IC device would provide the opportunity to protect a good device connected to the IC device when short circuit occurs.

- As per claim 16, Whetsel, Tsai et al. and Boomer teach the additional limitations.

Whetsel teaches that the predetermined BSR signals comprise a primary input buffer signal, an output BSR signal and a control BSR update register control signal ("FIGS. 4 and 6 illustrate exemplary output boundary scan cells according to the invention", col. 5, lines 24-25, Whetsel. "During Extest operation, the boundary scan cell receives Select 1 and Control 1 input to capture the IC output pin data into Mem1 and then shift it out for inspection via the serial output", col. 6, lines 52-55, Whetsel. "During Intest operation, Mux1 is controlled to input system data from the output of the latchable input buffer 103 to Mem1 for capturing and shifting out", fig. 15, col. 14, line 67 to col. 15, line 3, Whetsel).

- As per claim 17, Whetsel, Tsai et al. and Boomer teach the additional limitations.

Tsai et al. teach that the decision circuitry comprises exclusive OR circuitry operational to receive the primary input buffer signal and the output BSR signal ("The XOR gate 44 has a first input, which serves as a feedback input fb, a second input, which serves as a scan input, and an output", fig. 8, col. 6, lines 47-49, Tsai et al.).

- As per claim 18, Whetsel, Tsai et al. and Boomer teach the additional limitations.

Tsai et al. teach that the protection circuit register is further responsive to a previous protection data register (DR) associated with a corresponding protection DR chain to generate the second logic signal (fig. 5, col. 2, lines 29-32, Tsai et al.).

- As per claim 19, Whetsel, Tsai et al. and Boomer teach the additional limitations.

Whetsel teaches means responsive to the first logic signal, a test clock and a TAP controller instruction for generating a second logic signal; and means responsive to at least one BSR signal and the second logic signal for generating a protection circuit output control signal, wherein the protection circuit output control signal operates within one test clock cycle to disable circuit output associated with a short circuit corresponding to the IC device ("The invention relates to integrated circuits (ICs) and, more particularly, to boundary scan cells implemented at input and output pins of ICs to simplify testing of the ICs and their wiring interconnections", col. 1, lines 22-25, Whetsel. "Using the boundary scan cells of the present

invention in FIGS. 4 and 6, the latchable output buffer 40, when used in combination with the momentary control method of Control 2 (FIG. 4) or Control 2 and Transfer (FIG. 6), significantly reduces the time an output buffer can be forced into a short circuit condition. For example, the Control 2 or Control 2 and Transfer signals can be made to momentarily enable TG2 or TG2 and TG3 for only one half TCK period during update. After the momentary update enable goes away, the latch buffer provides feedback to correct for any output short condition immediately. In comparing short circuit correction times between the boundary scan cell of FIG. 3 (4 TCK periods) and those of FIGS. 4 and 6 (1/2 TCK period), the cells of the present invention correct shorts in 12.5% of the time it takes the prior art cell to correct shorts. Therefore the invention reduces the potential for output buffers to be degraded or destroyed during Extest or Intest operation. The reason for this improved short circuit protection provided by the invention is that the latchable output buffer 40 immediately and asynchronously corrects for logic differences between the input and the output of the output buffer using the latch buffer as a feedback mechanism", fig. 4, 6, col. 10, lines 7-28, Whetsel).

Tsai et al. teach means responsive to predetermined boundary scan register (BSR) signals and a test access port (TAP) controller mode signal for generating a first logic signal ("The boundary scan registers and the TAP controller", col. 3, lines 21-22, Tsai et al. "The XOR gate 44 has a first input, which serves as a feedback input fb, a second input, which serves as a scan input, and an output", fig. 8, col. 6, lines 47-49, Tsai et al.).

Boomer teaches disabling an output buffer associated with a short circuit corresponding to the IC device ("The step of tristating the output buffer circuit is accomplished by logically processing the short circuit sensing signal, generating a short circuit tristate enable signal SOEB, and coupling the short circuit tristate enable signal to the tristate enable input of the existing tristate enable circuit for tristating (i.e. disabling) the output buffer circuit", col. 2, lines 51-57, Boomer).

- As per claim 20, Whetsel, Tsai et al. and Boomer teach the additional limitations.

Tsai et al. teach that the means for generating a first logic signal comprises decision circuitry ("The XOR gate 44 has a first input, which serves as a feedback input fb, a second input, which serves as a scan input, and an output", fig. 8, col. 6, lines 47-49, Tsai et al.).

- As per claim 21, Whetsel, Tsai et al. and Boomer teach the additional limitations.

Whetsel teaches that the means for generating a second logic signal comprises a test protection circuit register ("If a short to ground existed on the IC output pin and the momentary control method were used to transfer a logic one from Mem1 to the latchable output buffer 40, the latchable output buffer would temporarily force (during the Control 2 or Control 2 and Transfer time) the output to a logic one. However, after the momentary control goes away, the latchable output buffer 40 would, due to the output feedback from the latch buffer, immediately switch from outputting a logic one to outputting a logic zero, thus removing the voltage contention at the IC output pin", col. 9, lines 30-39, Whetsel). The examiner would like to point out that Mem1 is a capture/shift memory such as a flip-flop, col. 1, line 35, Whetsel.

- As per claim 22, Whetsel, Tsai et al. and Boomer teach the additional limitations.

Tsai et al. teach that the test protection circuit register is further responsive to a previous protection data register (DR) associated with a corresponding protection DR chain to generate the second logic signal (fig. 5, col. 2, lines 29-32, Tsai et al.).

- As per claim 23, Whetsel, Tsai et al. and Boomer teach the additional limitations.

Whetsel teaches that the means for generating a protection circuit output control signal comprises logic circuitry ("Using the boundary scan cells of the present invention in FIGS. 4 and 6, the latchable output buffer 40, when used in combination with the momentary control method of Control 2 (FIG. 4) or Control 2 and Transfer (FIG. 6), significantly reduces the time an output buffer can be forced into a short circuit condition. For example, the Control 2 or Control 2 and Transfer signals can be made to momentarily enable TG2 or TG2 and TG3 for only one half TCK period during update. After the momentary update enable goes away, the latch buffer provides feedback to correct for any output short condition immediately. In comparing short circuit correction times between the boundary scan cell of FIG. 3 (4 TCK periods) and those of FIGS. 4 and 6 (1/2 TCK period), the cells of the present invention correct shorts in 12.5% of the time it takes the prior art cell to correct shorts. Therefore the invention reduces the potential for output buffers to be degraded or destroyed during Extest or Intest operation. The reason for this improved short circuit protection provided by the invention is that the latchable output buffer 40

immediately and asynchronously corrects for logic differences between the input and the output of the output buffer using the latch buffer as a feedback mechanism", fig. 4, 6, col. 10, lines 7-28, Whetsel).

- As per claim 24, Whetsel, Tsai et al. and Boomer teach the additional limitations.

Whetsel teaches that the predetermined BSR signals comprise a primary input buffer signal, an output BSR signal and a control BSR update register control signal ("FIGS. 4 and 6 illustrate exemplary output boundary scan cells according to the invention", col. 5, lines 24-25, Whetsel. "During Extest operation, the boundary scan cell receives Select 1 and Control 1 input to capture the IC output pin data into Mem1 and then shift it out for inspection via the serial output", col. 6, lines 52-55, Whetsel. "During Intest operation, Mux1 is controlled to input system data from the output of the latchable input buffer 103 to Mem1 for capturing and shifting out", fig. 15, col. 14, line 67 to col. 15, line 3, Whetsel).

- As per claim 25, Whetsel, Tsai et al. and Boomer teach the additional limitations.

Tsai et al. teach that the means for generating a first logic signal comprises exclusive OR circuitry operational to receive the primary input buffer signal and the output BSR signal ("The XOR gate 44 has a first input, which serves as a feedback input fb, a second input, which serves as a scan input, and an output", fig. 8, col. 6, lines 47-49, Tsai et al.).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 571-272-3822. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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